Amendments to the Specification:

Please replace the paragraph beginning at page 5, line 15 with the following amended paragraph:

First drive unit 54 includes a high DC write (direct current) signal (WDHX1) source 60, a low DC write signal (WDLX1) source 62, a high boost signal (BSTHX1) source 64 and a low boost signal (BSTLX1) source 66. First drive unit 54 responds to control unit 68 to selectively provide drive signals to a first connection locus 53 of write head 52. Second drive unit 56 includes a high DC write (direct current) signal (WDHX2) source 70, a low DC write signal (WDLX2) source 72, a high boost signal (BSTHX2) source 74 and a low boost signal (BSTLX2) source 76. Second drive unit 56 responds to control unit ~~68~~ 58 to selectively provide drive signals to a second connection locus 55 of write head 52.

Please replace the paragraph beginning at page 5, line 22 with the following amended paragraph:

High DC write signal source 60 is embodied in a first logic level current mirror 100. Low DC write signal source 62 is embodied in a second logic level current mirror 102. Current mirror 102 includes a diode-coupled transistor 104 in series with a transistor 106 between a signal input locus 105 and a lower voltage supply line 108 maintained substantially at a lower supply voltage V_{EE}. A direct current (DC) signal I_{WDC} is applied at signal input locus 105. Signal I_{WDC} establishes the direct current signal level for effecting data indications in write head 52. Current mirror 102 further includes transistors 110, 112 coupled in series between current mirror 100 and lower voltage supply line 108 and transistors 114, 116 coupled in series between current mirror 100 and lower voltage supply line 108. Preferably transistors 104, 110, 114 are bipolar transistors and transistors 106, 112, 116 are metal oxide silicon (MOS) transistors. A bias signal V_{REF1} gates transistors 106, 112 so that current signal I_{WDC} is permitted to flow through transistors 104, 106. That causes current signal I_{WDC} to be mirrored (biased toward

lower voltage signal V_{EE}) in the circuit segment including transistors 110, 112. Transistor 116 is gated by control unit 58 in response to data signals 80 applying a gating signal WDLX1 to gate locus 117 via network 68 (not shown in detail in FIG. 2) so that current signal I_{WDC} (biased toward lower voltage signal V_{EE}) also is mirrored in the circuit segment including transistors 114, 116. When control unit 58 gates transistor 116 to conduct, current signal I_{WDC} (biased toward lower voltage signal V_{EE}) is applied via junctions 120, 122 and network 78 to first connection locus 53 of write head 52.

Please replace the paragraph beginning at page 6, line 25 with the following amended paragraph:

High boost signal source 64 is embodied in a primary current mirror 150 operating with a secondary current mirror 154 (a first boost current mirror). Low boost signal source 66 is embodied in primary current mirror 150 operating with a secondary current mirror ~~154~~ 156 (a second boost current mirror).

Please replace the paragraph beginning at page 7, line 1 with the following amended paragraph:

Primary current mirror 150 includes a diode-coupled transistor 160 in series with a transistor 162 between a signal input locus 165 and an upper voltage supply line 138 maintained substantially at an upper supply voltage V_{CC}. A boost current reference signal I_{BSTREF} is applied at signal input locus 165. Boost signal I_{BSTREF} establishes the boost signal level for effecting data indications in write head 52. Current mirror ~~100~~ 150 further includes a diode connected transistor 164 coupled in series with transistors 166, 168 between lower voltage supply line 108 and upper voltage supply line 138 via a transistor 169. Preferably transistors 160, 164, 166 are bipolar transistors and transistors 162, 168, 169 are metal oxide silicon (MOS) transistors. Transistors 162, 168 are gated by bias signal V_{REF2}. Bias signal V_{REF1} gates transistor 169 so that boost signal I_{BSTREF} is permitted to flow through transistors 164, 166, 168, 169. Transistors 160, 162, 166,

168 cooperate to mirror boost signal I_{BSTREF} (biased toward upper voltage signal V_{CC}) to flow through transistors 170, 172 when transistor 172 is gated to conduct. Transistor 164 cooperates with transistors 160, 162, 166, 168 cooperate to mirror boost signal I_{BSTREF} (biased toward lower voltage signal V_{EE}) to flow through transistors 174, 176 when transistor 176 is gated to conduct. Transistor 176 is gated by control unit 58 in response to data signals 80 applying a gating signal BSTLX1 to gate locus ~~117~~ 177 via network 68 (not shown in detail in FIG. 2) so that boost signal I_{BSTREF} (biased toward lower voltage signal V_{EE}) flows through transistors 174, 176 and is applied via junction 122 and network 78 to first connection locus 53 of write head 52. Transistor 172 is gated by control unit 58 in response to data signals 80 applying a gating signal BSTHX1 to gate locus 173 via network 68 (not shown in detail in FIG. 2) so that boost signal I_{BSTREF} (biased toward ~~lower voltage signal V_{EE}~~ higher voltage signal V_{CC}) flows through transistors 170, 172 and is applied via junction 122 and network 78 to first connection locus 53 of write head 52.

Please replace the paragraph beginning at page 7, line 25 with the following amended paragraph:

Second drive unit 56 includes a high DC write (direct current) signal (WDHX2) source 70, a low DC write signal (WDLX2) source 72, a high boost signal (BSTHX2) source 74 and a low boost signal (BSTLX2) source 76. Second drive unit 56 responds to control unit ~~68~~ 58 to selectively provide drive signals to a second connection locus 55 of write head 52.

Please replace the paragraph beginning at page 8, line 1 with the following amended paragraph:

Low DC write signal source 70 is embodied in a current mirror 200. Low DC write signal source 72 is embodied in a current mirror 202. Current mirror 202 includes a diode-coupled transistor 204 in series with a transistor 206 between a signal input locus

205 and a lower voltage supply line 208 maintained substantially at a lower supply voltage V_{EE}. A direct current (DC) signal I_{WDC} is applied at signal input locus 205. Signal I_{WDC} establishes the direct current signal level for effecting data indications in write head 52. Current mirror 202 further includes transistors 210, 212 coupled in series between current mirror 200 and lower voltage supply line 208 and transistors 214, 216 coupled in series between current mirror 200 and lower voltage supply line 208. Preferably transistors 204, 210, 214 are bipolar transistors and transistors 206, 212, 216 are metal oxide silicon (MOS) transistors. A bias signal V_{REF1} gates transistors 206, 212 so that current signal I_{WDC} is permitted to flow through transistors 204, 206. That causes current signal I_{WDC} to be mirrored (biased toward lower voltage signal V_{EE}) in the circuit segment including transistors 210, 212. Transistor 216 is gated by control unit 58 in response to data signals 80 applying a gating signal WDLX2 to gate locus 217 via network 68 (not shown in detail in FIG. 2) so that current signal I_{WDC} (biased toward lower voltage signal V_{EE}) also is mirrored in the circuit segment including transistors 214, 216. When control unit 58 gates transistor 216 to conduct, current signal I_{WDC} (biased toward lower voltage signal V_{EE}) is applied via junctions 220, 222 and network ~~78~~ 79 to second connection locus 55 of write head 52.

Please replace the paragraph beginning at page 9, line 6 with the following amended paragraph:

High boost signal source 74 is embodied in a primary current mirror 250 operating with a secondary current mirror 252. Low boost signal source 76 is embodied in primary current mirror 250 operating with a secondary current mirror 256.

Please replace the paragraph beginning at page 9, line 9 with the following amended paragraph:

Primary current mirror 250 includes a diode-coupled transistor 260 in series with a transistor 262 between a signal input locus 265 and an upper voltage supply line 238

maintained substantially at an upper supply voltage V_{CC}. A boost current reference signal I_{BSTREF} is applied at signal input locus 265. Boost signal I_{BSTREF} establishes the boost signal level for effecting data indications in write head 52. Current mirror ~~200~~ 250 further includes a diode connected transistor 264 coupled in series with transistors 266, 268 between lower voltage supply line 208 and upper voltage supply line 238 via a transistor 269. Preferably transistors 260, 264, 266 are bipolar transistors and transistors 262, 268, 269 are metal oxide silicon (MOS) transistors. Transistors 262, 268 are gated by bias signal V_{REF2}. Bias signal V_{REF1} gates transistor 269 so that boost signal I_{BSTREF} is permitted to flow through transistors 264, 266, 268, 269. Transistors 260, 262, 266, 268 cooperate to mirror boost signal I_{BSTREF} (biased toward upper voltage signal V_{CC}) to flow through transistors 270, 272 when transistor 272 is gated to conduct. Transistor 264 cooperates with transistors 260, 262, 266, 268 cooperate to mirror boost signal I_{BSTREF} (biased toward lower voltage signal V_{EE}) to flow through transistors 274, 276 when transistor 276 is gated to conduct. Transistor 276 is gated by control unit 58 in response to data signals 80 applying a gating signal BSTLX2 to gate locus 277 via network 68 (not shown in detail in FIG. 2) so that boost signal I_{BSTREF} (biased toward lower voltage signal V_{EE}) flows through transistors 274, 276 and is applied via junction 222 and network 79 to second connection locus 55 of write head 52. Transistor 272 is gated by control unit 58 in response to data signals 80 applying a gating signal BSTHX2 to gate locus 273 via network 68 (not shown in detail in FIG. 2) so that boost signal I_{BSTREF} (biased toward ~~lower voltage signal V_{EE}~~ higher voltage signal V_{CC}) flows through transistors 270, 272 and is applied via junction 222 and network 79 to second connection locus 55 of write head 52.

Please replace the paragraph beginning at page 10, line 5 with the following amended paragraph:

Control unit 58 receives data signals 80 and responds to those received data signals to select which of transistors 116, 136, 172, 176, 216, 236, 272, 276 should be

activated for providing a signal to write head 52. DC write signals and boost signals are provided to connection locus 53 via a network 78 by gating selected of transistors 116, 136, 172, 176. DC write signals and boost signals are provided to connection locus 55 via a network 79 by gating selected of transistors 216, 236, 272, 276. An impedance matching circuit or unit ~~42~~ 82 is preferably coupled across write head 52 to match impedance of write head 52 with other components of apparatus 50.